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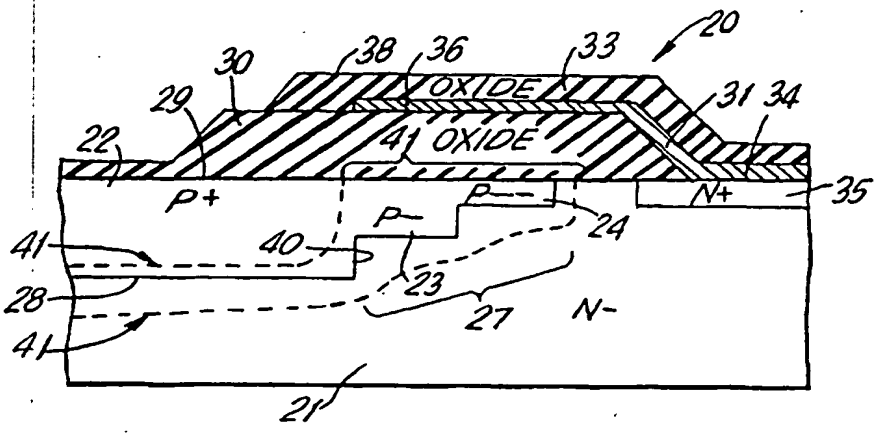

(57) Abstract

An integrated circuit (IC) (20) is formed on a semiconductor substrate (21). The IC has a PN junction (28) and a graded junction termination (27). A reverse field plate (31) is mounted adjacent the junction termination. One end of the field plate is mounted on and electrically connected to the substrate; the remainder of the field plate extends over a passivating oxide layer (30) which covers the substrate surface (29) adjacent the junction termination. The field plate provides a common potential surface which maintains a fixed potential on the substrate surface at the junction termination.

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A REVERSE FIELD PLATE, JUNCTION-TERMINATING STRUCTURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to the field of solid state electronics and, particularly, to a method of fabricating a semiconductor device and a device so formed.

2. Description of the Existing Art

Typical semiconductor device manufacturing processes produce junctions between differently doped portions of a semiconductor substrate. Various arrangements of these differently doped portions form specific types of semiconductor devices such as diodes, transistors, and the like. FIG. 1 shows a cross-section of a portion of semiconductor device 10 having PN junction 11 which is formed when a layer of P^+ doped material is deposited into substrate 12 of N^- doped material. Specifically, junction 11 is formed between N^- substrate 12 and P^+ layer 13.

Typically, during use of device 10 junction 11 alternatingly becomes forward and reversed biased as a result of a biasing voltage ± V. When junction 11 is reverse biased, the biasing voltage generates a relatively large electric field across the junction. Furthermore, the reverse bias forms a relatively wide transition region 14 within which the electric field is generated. However, transition region 14 does not have uniform width along the length of junction 11. For example, in those semiconductor devices where a diffused layer ends abruptly at a planar surface, the transition region is significantly narrower near the planar surface

of the semiconductor substrate than within the substrate. Such narrowing of the transition region is caused by a natural accumulation of positive charges on oxide layer 17 (assuming for the moment that plate 18 and oxide layer 19 are not part of device 10). This case is depicted in FIG. 1 by dashed lines A and B. Specifically, if P^+ layer 13 ends abruptly so that junction 11 follows dashed line A, the boundary of transition region 14 would follow dashed line B. Since the electric field is bounded by transition region 14, the electric field across junction 11 is much greater near the semiconductor surface than is the electric field across junction 11 within semiconductor 12. In some device applications, the reverse bias voltage and its corresponding electric field can become large enough to cause junction breakdown near the surface of the semiconductor substrate while that same magnitude voltage has no effect upon the junction within the semiconductor substrate.

To avoid junction breakdown, the transition region near the surface of the substrate is typically graded to widen the transition region at the planar surface. Graded junctions are implemented by diffusing a relatively lightly doped material (doped lighter than the P^+ material) at the junction and near the semiconductor surface. For the FIG. 1 example, junction 11 is formed between N^- substrate 12 and P^+ layer 13, P^- layer 15 and P^- layer 16. As such, the boundary of transition region 14 follows dashed line C. In this manner, transition region 14 is widened to lessen the electric field across junction 11 near the substrate surface. Such graded junctions are known in the art as graded termination structures. Typically, to complete the device, the termination structure as well as the semiconductor device surface is coated with insulating or passivating layer 17.

This termination technique reduces premature junction breakdown by gradually reducing the voltage at the surface over a wide transition region, thereby avoiding abrupt potential changes at the substrate surface. Essentially, a graded junction termination is designed so that the electric field at the surface is distributed over a wide transition region. However, a graded termination can be susceptible to surface charges both in and on the passivating or insulating material forming the passivating layer. Such surface charges, which can be the result of dust, water vapor, surface impurities, and the like that fall upon the substrate during processing, can alter and distort the desired electric-field distribution at the substrate surface. The electric field distortion can cause abrupt potential changes at the substrate surface, thus limiting the effect of the graded junction termination. Such abrupt potential changes cause currents, possibly in destructive amounts, to flow through the termination structure. Consequently, surface charges near a graded termination can significantly contribute to premature junction breakdown.

To render graded junction terminations less susceptible to surface charges, so-called field plates are mounted over the passivating layer and adjacent the termination structure. FIG. 1 shows conventional field plate 18, which is a conductive member having one end shorted to P^+ layer 13 and its other end extending over passivating layer 17 above the graded termination structure formed by P^+ layer 13, P^- layer 15 and P^{--} layer 16. In this manner, field plate 18 has the same potential as P^+ layer 13. Hence, conductive field plate 18 provides a uniform potential which is superimposed over the graded junction termination. The presence of this uniform potential "stabilizes" the junction termination by fixing the potential at the substrate surface. Surface charges that accumulate on

passivating layer 19, which is formed above field plate 18, cannot penetrate the field plate. As a result, field plate 18 renders the junction termination less susceptible to premature breakdown due to surface charge.

Although the use of field plates has generally served the purpose, it has not always been an acceptable solution to surface charge induced junction breakdown for at least two reasons. First, access to the diffused layer (e.g., P^+ layer 13) for mounting a field plate may not always be practical or possible due to circuit layout or device complexity. Second, because the field plates are individually shorted to surfaces (diffused layers) that carry relatively high voltages which vary with respect to one another, the field plates must be properly spaced from one another to obtain sufficient electrical isolation between adjacent plates. This requirement can be a significant drawback when a large number of field plates is to be mounted on a common substrate in close proximity to one another.

SUMMARY OF THE INVENTION

To remedy the deficiencies in the art, the present invention teaches the use of a unique reverse field plate, junction-terminating structure and a method of fabricating such a field plate. The invention reverses the orientation of a field plate (hereinafter referred to as a "reverse" field plate) with respect to the termination structure as compared to that employed in the aforementioned existing art.

Specifically, the reverse field plate is connected (shorted) to the semiconductor substrate rather than a diffused layer as in the existing art. As such, the reverse field plate does not occupy surface area above the diffused layer. Consequently, the surface area above the diffused layer may be used for placement of

other, more complex semiconductor structures. Also, by connecting several closely spaced reverse field plates to the substrate, the reverse field plates are all maintained at a substantially common potential level, thereby making electric isolation of the plates less critical than in the prior art.

These features arising from the use of the invention advantageously permit a greater component density to be achieved on the semiconductor substrate, thereby solving one of the most critical problems confronting integrated circuit designers, viz. reduction of integrated circuit size.

In one embodiment, the present invention comprises a semiconductor device having a semiconductor substrate with a layer of doped impurities (diffused layer) extending a predetermined depth from the surface into the substrate to form a semiconductor junction and a junction termination. An insulating layer is formed on the surface of the substrate and covers the junction termination. A conductive plate has a first portion electrically connected to the substrate at a location spaced laterally from the layer of doped impurities, and a second portion extending over the insulating layer adjacent the junction termination. The potential of the conductive plate, essentially equivalent to the potential of the substrate, is superimposed on the junction termination to "stabilize" the surface potential.

In a second embodiment, the present invention includes an integrated circuit which is formed on a semiconductor substrate. The integrated circuit includes a PN junction and a graded junction termination. A reverse field plate is mounted adjacent the junction termination. One portion of the field plate is electrically connected to the substrate; another portion of the field plate extends over a passivating oxide layer

which covers the substrate surface adjacent the junction termination. The field plate provides a potential surface which maintains a fixed potential on the substrate surface at the junction termination.

In both embodiments, since the potential on the conductive field plate is essentially equivalent to the potential of the substrate, electrical isolation of multiple plates on a common substrate is accomplished using relatively small spacings between plates.

Additionally, the present invention is directed to a semiconductor fabrication method wherein a PN junction having a graded termination structure is diffused into a semiconductor substrate. A passivating layer is formed on a surface of the substrate adjacent the termination structure. A conductive field plate is deposited such that a first portion of the conductive field plate is deposited on the substrate while a second portion is deposited over the passivating layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The teachings of the invention can be readily understood by considering the following detailed description in conjunction with the accompanying drawing, in which:

FIG. 1 is a cross-sectional view of a portion of an existing semiconductor device.

FIG. 2 is a cross-sectional view of a portion of semiconductor integrated circuit 20 fabricated in accordance with the present invention and taken along lines 2-2 shown in FIG. 3; and

FIG. 3 depicts a top plan view of the portion of semiconductor integrated circuit 20 depicted in FIG. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

To best understand the invention, it is recommended that the reader simultaneously refer to both FIGs. 2 and 3 while reading the following description.

Typically, a simple semiconductor device contains a substrate of one type of semiconductor material and a layer diffused therein formed of another type of semiconductor material. Additionally, a graded junction termination is typically formed near the surface of the substrate, along a junction between the substrate and the diffused layer. A passivating layer is formed over, at least, the graded junction termination. In general, the inventive method forms a field plate that is electrically connected at one end to the substrate and the other end of the field plate extends over the passivating layer. The passivating layer electrically insulates the field plate from the junction termination. Another (second) passivating layer is then formed over the field plate. In operation, the field plate isolates any surface charges that accumulate on the passivating layer from distorting the electrical characteristics of the junction termination.

Specifically, FIG. 2 depicts a cross-section of a portion of integrated circuit 20 having semiconductor substrate 21 which is lightly doped with N type impurities. FIG. 3 depicts a top plan view of the portion of integrated circuit 20 depicted in FIG. 2.

As shown, P^+ layer 22 is formed by highly doping upper surface 29 of substrate 21 to form PN junction 28. At terminating end 40 of P^+ layer 22, a graded junction

termination 27 is formed by grading and decreasing the P type impurities to form two graded regions, e.g., P^- region 23 and P^{--} region 24. Specifically, P^- region 23 is formed by moderately doping a relatively small region of surface 29 adjacent end 40 of layer 22 with P type impurities such that the impurity concentration and layer thickness are less than that of layer 22. Likewise, P^{--} region 24 is formed by lightly doping another relatively small region of surface 29 adjacent P^- region 23 with P type impurities such that the impurity concentration and layer thickness are less than that of P^- region 23. A passivating oxide layer 30 is formed on a portion of surface 29 to at least cover junction termination 27.

PN junction 28 may be used in integrated circuit 20 as a simple unijunction diode or, in conjunction with other semiconductor components (not shown), it may be part of a more complex device such as a silicon controlled rectifier, a bipolar transistor, a field effect transistor, and the like. In this regard, such other integrated components would be conventional and are located on either side of, or to the rear and front of the structure shown in FIG. 2. The placement of such other components are within the knowledge of those skilled in these arts.

Furthermore, the doping methods, used to fabricate layer 22 and regions 23 and 24, can include any conventional doping process including diffusion. Such diffusion can be performed in three steps as follows: first, P type impurities are lightly diffused to a first, shallow depth to form layer 22 and regions 23 and 24; next, region 24 is masked, and P type impurities are diffused to a deeper depth and at a higher concentration; and finally, regions 23 and 24 are masked, and P^+ layer 22 is formed by heavy diffusion of P type impurities to a greater depth. Of course, those skilled in the art can use other diffusion and/or doping methods based on the

present teachings to produce layer 22 and regions 23 and 24. Also, termination 27 can be graded continuously, as opposed to being graded in steps as described above.

When PN junction 28 is reverse biased, a relatively high potential difference can appear at surface 29 and across junction termination 27. Specifically, this potential difference extends across termination 27 from P^+ layer 22 to substrate 21. The graded configuration of termination 27 achieves so-called high-voltage, reverse-bias blocking by gradually reducing this high potential difference over relatively wide transition region 41. However, it is widely recognized that surface charges, which accumulate on passivating materials of an integrated circuit, adversely distort this gradual reduction of the surface potential. In particular, such surface charges interfere with the uniformity of the electric field across the transition region at the surface of the substrate. As such, the surface charges can cause the potential across the transition region to increase at certain points and decrease at others. Such fluctuations in potential may be detrimental to device operations and could lead to device failure. Specifically, those points of increased potential tend to generate excessive currents through the junction which cause junction breakdown. To prevent such surface charge induced breakdown, integrated circuit 20 includes conductive field plate 31 which superimposes a uniform surface potential upon termination 27.

Field plate 31 contains first portion 34 that is joined to surface 29 of N^- substrate 21 while second portion 36 of the field plate is deposited upon oxide layer 30. Field plate 31, which is formed of a conductive material such as polysilicon, extends over termination 27. Specifically, portion 36 of field plate 31 extends over the entire length of junction termination 27. Field plate 31 is passivated with

insulating oxide layer 33 having exterior surface 38. In FIG. 3, oxide layer 33 is not depicted such that the underlying field plate 31 is clearly depicted. Portion 34 of field plate 31 is joined to N^- substrate 21 via N^+ layer 35. In a well-known manner, the N type impurities of N^+ layer 35 can be diffused into surface 29 via a conventional diffusion process, or they can simply be created as a result of the application of conductive field plate 31 to substrate 21.

The orientation of field plate 31 is reversed from conventional practice inasmuch as the plate is mounted on and electrically connected to substrate 21 rather than on diffused layer 22 as conventionally taught. Field plate 31 operates to maintain a fixed potential on surface 29 in the area of termination 27. Also, any electric fields that are associated with surface charges that may accumulate on exterior surface 38 of oxide layer 33 cannot penetrate field plate 31. Consequently, field plate 31 is a surface potential stabilizing structure because the plate essentially shields termination 27 from the effects of surface charges.

The inventive teachings for fabricating and using a reverse field plate provides the integrated circuit designer with an additional field-plate mounting option. The invention may be used for plate mounting when access to a diffused layer, such as P^+ layer 22, is not practical, i.e., when additional layers are to be formed upon the diffused layer. Also, because all such field plates 31 on an integrated circuit (IC) are essentially at a common potential, i.e., the potential of substrate 21, electrical isolation of plates 31 is readily achieved. As such, in those situations where a number of field plates 31 are to be mounted on an integrated circuit, the plates can be spaced more closely to each other when using the invention than is usually

possible when each plate is connected to a different high-potential surface, e.g., a diffused layer. Decreasing required plate spacing has the important beneficial effects of decreasing device size and/or cost.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is to be understood, therefore, that within the scope of the appended claims, the present invention can be practiced otherwise than as specifically described.

What is claimed is:

1. A semiconductor device (20) comprising:

a semiconductor substrate (21) having a surface (29);

a layer (22, 23, 24) of doped impurities extending a predetermined depth from said surface into said substrate to form a semiconductor junction (28) and a junction termination (27);

an insulating layer (30) formed on said surface and covering said junction termination; and

a conductive plate (31) having a plate potential, said plate having a first portion (34) mounted on and electrically connected to said substrate at a location spaced from said layer of doped impurities and a second portion (36) extending over said insulating layer adjacent said junction termination, whereby said plate potential is superimposed on said junction termination.

2. The semiconductor device of claim 1 wherein said junction termination is a graded termination.

3. The semiconductor device of claim 2 wherein said graded termination includes first and second regions (23, 24) of doped impurities, each said region having different impurity concentrations and different depths.

4. A semiconductor device (20) comprising:

an N^- substrate (21) having a surface (29);

a layer (22, 23, 24) of P type impurities extending a predetermined depth from said surface into said substrate to form a PN junction (28) and a junction termination (27);

an insulating layer (30) formed on said surface and covering said junction termination; and

a conductive plate (31) having a plate potential, said plate having a first portion (34) mounted on and electrically connected to said substrate at a location

spaced from said layer of P type impurities and a second portion (36) extending over said insulating layer adjacent said junction termination, whereby said plate potential is superimposed on said junction termination.

5. The semiconductor device of claim 4 wherein said junction termination is a graded termination.

6. The semiconductor device of claim 5 wherein said graded termination includes at least two regions (24, 23) of P type impurities, said regions having different predetermined impurity concentrations and different predetermined depths from one another.

7. The semiconductor device of claim 6 wherein said layer of P type impurities has at least one heavily doped P^+ region (22) which forms said PN junction and at least one lightly doped P^{--}region (24) which forms said junction termination.

8. The semiconductor device of claim 7 wherein said junction termination further includes a lightly doped P^- region (23), and said P^- region is located between said P^+ region and said P^{--}region.

9. The semiconductor device of claim 8 wherein said predetermined depth is such that said P^- region is deeper than said P^{--} region and is shallower than said P^+ region.

10. The semiconductor device of claim 9 wherein said conductive plate is polysilicon.

11. A method of fabricating a semiconductor device comprising:

forming a PN junction having a termination structure on a semiconductor substrate;

forming a passivating layer adjacent said termination structure; and

depositing a first portion of a conductive field plate on said substrate and depositing a second portion of said conductive field plate on said passivating layer in superimposed relation to said termination structure.

12. The method of claim 11 wherein said termination structure is a graded termination structure.

13. A method of fabricating a semiconductor device comprising:

diffusing a layer of doped impurities into a surface of a semiconductor substrate to a predetermined depth and forming a semiconductor junction and a junction termination;

forming an insulating layer on said surface to cover said junction termination; and

forming a field plate having a plate potential including depositing a first portion of a conductive plate on said substrate at a location spaced from said layer of doped impurities and a second portion of said conductive plate on said insulating layer adjacent said junction termination, whereby said plate potential is superimposed on said junction termination.

14. The method of claim 13 wherein said junction termination is a graded junction termination.

15. A method of fabricating a semiconductor device comprising:

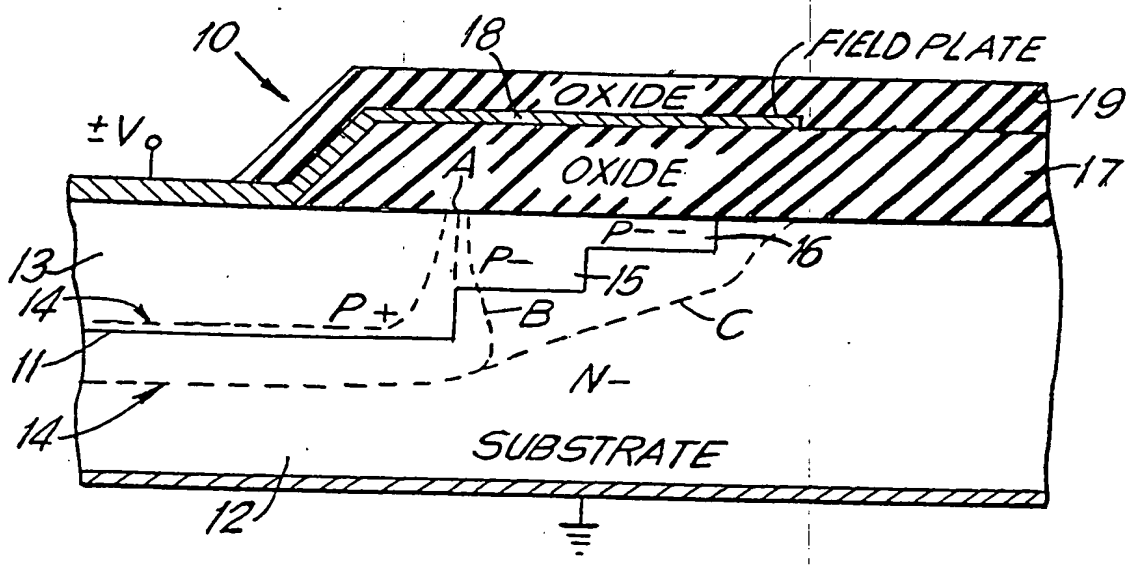
diffusing a layer of P type impurities into a surface of an N^- substrate for a predetermined depth to form a PN junction and a junction termination;

forming an insulating layer on said surface to cover said junction termination; and

forming a reverse field plate having a plate potential by depositing a first portion of a conductive plate on said substrate at a location spaced from said layer of P type impurities and a second portion of said

conductive plate on said insulating layer adjacent said junction termination, whereby said plate potential is superimposed on said junction termination.

16. The method of claim 15 wherein said junction termination is a graded termination.



(PRIOR ART)

FIG. 1

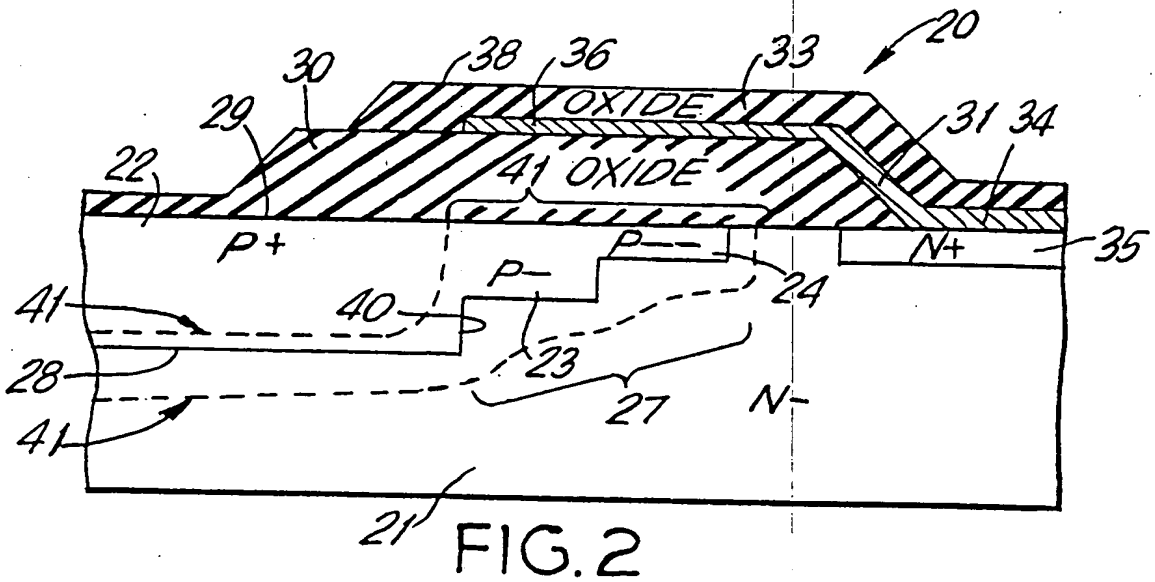


FIG. 2

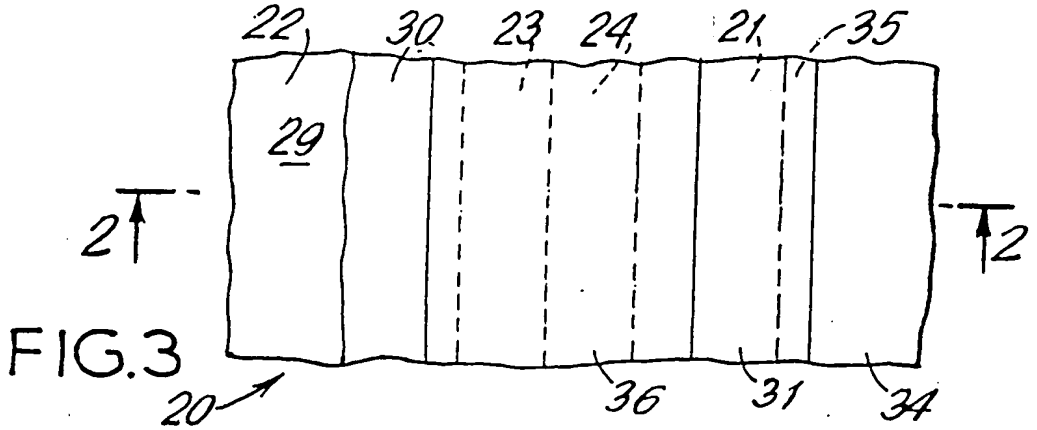


FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 94/06315

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L29/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol.36, no.4, April 1989, NEW YORK US pages 651 - 658 LALITA MANCHADA ET AL 'A High-Performance Directly Insertable Self-Aligned Ultra-Rad-Hard and Enhanced Isolation Field-Oxide Technology for Gigahertz Silicon NMOS/CMOS VLSI'	1,4
Y	see the whole document ---	1-16
Y	US,A,4 172 260 (OKABE ET AL) 23 October 1979 see the whole document ---	1-16
X	BE,A,656 774 (V. H. GRINICH ET AL) 1 April 1965 see the whole document ---	1,4,11, 13,15
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
19 October 1994	14. 11. 94

Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IEEE TRANSACTIONS ON CONSUMER ELECTRONICS, vol.CE-26, no.3, August 1980, NEW YORK US pages 367 - 374 ICHIRO IMAIZUMI ET AL 'NOVEL IC STRUCTURE FOR 150V HIGH-VOLTAGE CONSUMER IC' see page 171, column 1; figure 7B ---	1,2,4,5
X	PATENT ABSTRACTS OF JAPAN vol. 5, no. 176 (E-081) 13 November 1981 & JP,A,56 103 463 (YAMAOKA MASAMI) 18 August 1981 see abstract -----	1

ERNATIONAL SEARCH REPORT

Information on patent family members

Inter mal Application No
PCT/US 94/06315

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-4172260	23-10-79	JP-C- 1031985	29-01-81
		JP-A- 53068581	19-06-78
		JP-B- 55025513	07-07-80
		DE-A,B,C 2753613	08-06-78
		NL-A- 7713333	05-06-78
BE-A-656774	01-04-65	CH-A- 456773	
		FR-A- 1419107	
		NL-A- 6413894	05-08-65